

IN THE CLAIMS

Please cancel claims 1-21, without prejudice.

22. (Original) A computer system comprising:
- a bus;
- a processor coupled to the bus;
- a nonvolatile memory device coupled to the bus to receive commands from the processor, the commands including an increment command, the non volatile memory device including:
- a nonvolatile storage array organized in digits having non-uniform bases;
- and
- circuitry to increment a count value represented by the digits in response to the increment command.
23. (Original) A computer system comprising:
- a bus;
- a processor coupled to the bus;
- a security co-processor coupled to the bus to receive commands and data from the processor; and
- a nonvolatile memory device coupled to receive commands from the security co-processor, the commands including an increment command, the nonvolatile memory device including
- a nonvolatile storage array organized in digits having non-uniform bases;
- and

circuitry to increment a count value represented by the digits in response to the increment command.

24. (Original) A method comprising:
 - receiving a command to increment a counter implemented in a nonvolatile storage device, the nonvolatile storage device including a nonvolatile storage array organized in digits that have non-uniform bases, the digits defining the counter;
 - searching each of the digits in order of significance until a least significant unprogrammed bit of one of the digits is found; and
 - programming the unprogrammed bit to carry out the increment command.
25. (Original) The method of claim 24 further comprising erasing bits of each of the digits less significant than the one of the digits containing the unprogrammed bit to carryout the increment command.
26. (Original) The method of claim 24 further comprising receiving a command specifying a base for each of the digits of the counter.
27. (Original) The method of claim 24 further comprising receiving a command specifying a quantity of the digits.

Please add the following new claims:

- 1 28. (New) The computer system of claim 22 wherein the nonvolatile storage includes
- 2 a plurality of blocks of storage cells, each of the digits being stored in a respective one of
- 3 the blocks.
- 1 29. (New) The computer system of claim 28 wherein one of the digits spans two or
- 2 more of the blocks.
- 1 30. (New) The computer system of claim 28 wherein the nonvolatile storage is a
- 2 flash erasable programmable read only memory in which a selected block of the plurality
- 3 of blocks is erased in response to an erase command that identifies the selected block.
- 1 31. (New) The computer system of claim 22 wherein each of the digits include
- 2 includes a respective number of bits according to its base.
- 1 32. (New) The computer system of claim 31 wherein the number of bits is equal to
- 2 the base minus one.
- 1 33. (New) The computer system of claim 31 wherein the circuitry to increment the
- 2 count value comprises circuitry to increment one digit of the digits by
- 3 programming only one bit of the digit.
- 1 34. (New) The computer system of claim 33 wherein the circuitry to increment the
- 2 one digit of the digits comprises circuitry to evaluate bits of the one digit to
- 3 identify a least significant bit of the one digit that is in an erased state, the least
- 4 significant bit being the only one bit programmed to increment the one digit.

1 35. (New) The computer system of claim 22 wherein the circuitry includes circuitry
2 to increment one of the digits and to erase each of the digits less significant than the one
3 of the digits.

1 36. (New) The computer system of claim 35 wherein the circuitry to erase each of
2 the digits less significant than the one of the digits comprises circuitry to concurrently
3 erase each of the digits less significant than the one of the digits.

1 37. (New) The computer system of claim 22 further comprising:
2 program circuitry to write data to the nonvolatile storage in response to
3 program commands received from an external source; and
4 circuitry to detect whether an address specified by one of the program
5 commands falls within a range of the nonvolatile storage allocated to
6 the digits and, if so, to disallow the program circuitry from writing data at
7 the address.

1 38. (New) The computer system of claim 37 further comprising circuitry to output
2 the count value represented by the digits in response to the increment command.

1 39. (New) The computer system of claim 37 further comprising circuitry to output
2 the count value represented by the digits in response to a read command.

1 40. (New) The computer system of claim 37 further comprising circuitry to generate
2 a binary representation of the count value for output to the processor.

1 41. (New) The computer system of claim 40 wherein the circuitry to generate a
2 binary representation of the count value is configured to generate a distinct binary
3 representation of the value of each of the digits.